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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,030	07/28/2003	Jung-Chih Kuo	10112601	7372

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QUINTERO LAW OFFICE
1617 BROADWAY, 3RD FLOOR
SANTA MONICA, CA 90404

EXAMINER	
YOUNG, CHRISTOPHER G	
ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,030	KUO ET AL.	
	Examiner	Art Unit	
	Christopher G. Young	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *6-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Bode et al., US Patent Number 6,737,208.

The instant application claims are drawn to An exposure system with group compensation, comprising: a lot classification database to record a group classification of at least one lot wafer; a compensation unit to obtain the group classification of the lot wafer from the lot classification database, retrieve a group compensation value according to the group classification, and compensate at least one overlay parameter according to the group compensation value; and a first exposure device to perform a back-end process including overlay and exposure processes on the lot wafer using the compensated overlay parameters.

Bode et al. describe, teach and suggest all the claimed embodiments of the instant application. Bode et al. describe a processing line 100 also includes an overlay metrology tool 130 adapted to determine overlay errors in photoresist patterns formed by the photolithography tool 120. In general, the overlay metrology tool 130 may be any type of tool capable of measuring overlay error.

A controller 140 is provided for controlling the stepper 124 based on feedforward overlay metrology data collected by the overlay metrology tool 130. In some embodiments, the controller 140 may control the stepper 124 based on both feedforward and feedback overlay metrology data. A data store 150 is provided for storing overlay metrology data regarding the wafers 110 measured by the overlay metrology tool 130. The overlay metrology data may be stored and indexed by wafer lot ID. Of course, the process line 100 may include multiple photolithography tools 120

collecting overlay data and multiple overlay metrology tools 130 with shared or individual controllers 140.

Referring to FIG. 1, the process employed by the controller 140 for determining control actions for the photolithography tool 120 is described in more detail. In general, the controller 140 considers overlay error data from previous layers when determining the overlay settings for the stepper 124 for a current layer. This consideration of previous overlay error measurements is referred to herein as a feedforward control technique. Depending on the particular implementation, the controller 140 may determine control actions for individual wafers or for lots of wafers. If control is performed on a lot level, the feedforward overlay error data may be associated with one or more wafers in the lot that were measured. If control is performed on a wafer level, each wafer may have an associated feedforward overlay error measurement. Of course different degrees of granularity may be used. For example, an averaging or interpolation technique may be used for wafers without specific feedforward overlay error data available.

Prior to processing a selected wafer in the photolithography tool 120, the controller 140 accesses the data store 150 to determine the overlay error measured for the previous process layer. When the controller 140 determines that an overlay error condition corresponding to an overlay control input signal is not inside the deadband, the feedforward and feedback overlay errors are used to update that overlay control input signal for a photolithography process performed on the current wafer, a subsequent wafer within the lot, or a subsequent lot of wafers. The controller 140

determines a step size for changing in the value of the overlay control input signal in accordance with a control model. Equation 1 below provides an exemplary control equation for determining a change to an overlay control input signal.

3. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Jones et al., US Patent Number 6,815,232.

The instant application claims are drawn to An exposure system with group compensation, comprising: a lot classification database to record a group classification of at least one lot wafer; a compensation unit to obtain the group classification of the lot wafer from the lot classification database, retrieve a group compensation value according to the group classification, and compensate at least one overlay parameter according to the group compensation value; and a first exposure device to perform a back-end process including overlay and exposure processes on the lot wafer using the compensated overlay parameters.

Jones et al. describe, teach and suggest the claimed embodiments of the instant application. Referring to FIG. 2, a simplified diagram of an illustrative processing line 200 for processing wafers 210 in accordance with one illustrative embodiment of the present invention is provided. The processing line 200 includes a photolithography tool 220 for forming a pattern in a photoresist layer formed on the wafer 210. The photolithography tool 220 includes a track 222 coupled to a stepper 224. The track 222 spins photoresist material onto the wafer 210 and pre-bakes the photoresist layer.

The processing line 200 also includes an overlay metrology tool 230 adapted to determine overlay errors in photoresist patterns formed by the photolithography tool 220.

A controller 240 is provided for controlling the stepper 224 based on overlay metrology data collected by the overlay metrology tool 230. A data store 250 may be provided for storing overlay metrology data regarding the wafers 210 measured by the overlay metrology tool 230. For example, the overlay metrology data may be stored and indexed by wafer ID and/or lot ID, depending on the granularity available. Of course, the process line 200 may include multiple photolithography tools 220 collecting overlay data and multiple overlay metrology tools 230 with a shared or individual controllers 240.

When the stepper 224 completes processing of a wafer 210, the wafer 210 is examined by the overlay metrology tool 230. The wafer may be examined prior to developing of the photoresist layer (i.e., using the latent photoresist image) or after the developing process (i.e., using the photoresist pattern). The overlay metrology tool 230 provides a measurement of misregistration that was present in the previous exposure step. The overlay metrology tool 230 incorporates multiple overlay targets on multiple underlying process layers for measuring the misregistration. In this manner, the controller 240 may align the photoresist layer with multiple underlying process layers.

The overlay metrology tool 230 stores the overlay error for the measured wafer 210 in the data store 250. The overlay error metrology data may be indexed by wafer/lot ID and layer. Returning to FIG. 2, the process employed by the controller 240

for determining control actions for the photolithography tool 220 is described in more detail. In general, the controller 240 considers overlay error data measured using both of the pairs 380, 390 of overlay targets. Depending on the particular implementation, the controller 240 may determine control actions for individual wafers or for lots of wafers. If control is performed on a lot level, the overlay error data may be associated with one or more wafers in the lot that were measured. If control is performed on a wafer level, each wafer may have an associated overlay error measurement.

Of course different degrees of granularity may be used. For example, an averaging or interpolation technique may be used for wafers without specific feedforward overlay error data available.

The controller 240 may adjust the recipe of the stepper 224 for a current wafer as well as for subsequent wafers based on the overlay error data. The controller 240 may be configured with a deadband range, in which no corrections are made. The overlay errors may be compared to a predetermined set of threshold parameters. In one embodiment, the deadband contains a range of error values associated with control input signals centered proximate a set of corresponding predetermined target values. If the overlay errors acquired from the overlay metrology tool 230 are smaller than their corresponding predetermined threshold values, that particular error is deemed to be in the deadband, and the controller 240 makes no changes to the overlay control inputs. A primary purposes of the deadband is to prevent excessive control actions from causing the semiconductor manufacturing process to be inordinately jittery.

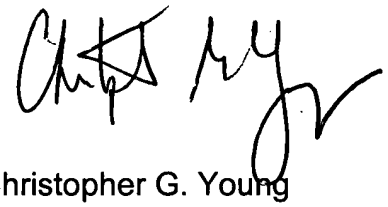
When the controller 240 determines that an overlay error condition corresponding to an overlay control input signal is not inside the deadband, the overlay errors are used to update that overlay control input signal for a photolithography process performed on the current wafer, a subsequent wafer within the lot, or a subsequent wafer or lot of wafers. The controller 240 determines a step size for changing in the value of the overlay control input signal in accordance with a control model. Equation 1 below provides an exemplary control equation for determining a change to an overlay control input signal.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher G. Young whose telephone number is 571-272-1394. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Christopher G. Young
Primary Examiner
Art Unit 1756

cgy